Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims

1. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including a selectable number of taps, wherein the equalization implementation circuitry operates on the received data signal;

programmable circuitry for allowing a first number of taps to be specified;

processing circuitry for computing a second number of taps; and

selection circuitry for selecting one of the first and second numbers as the selectable number, wherein the selection circuitry is programmed to select only once while the equalization implementation circuitry operates on the received data signal.

2. (original) The circuitry defined in claim 1 wherein the selection circuitry is programmable to make its selection.

3. (original) The circuitry defined in claim 1 wherein the processing circuitry performs an algorithm to compute the second number.

4. (original) A digital processing system comprising:

processor circuitry;

a memory coupled to the processor circuitry; and

programmable logic device circuitry as defined in claim 1 coupled to the processor circuitry and the memory.

5. (original) A printed circuit board on which is mounted programmable logic device circuitry as defined in claim 1.

6. (original) The printed circuit board defined in claim 5 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry.

7. (original) The printed circuit board defined in claim 5 further comprising:

processor circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry.

8. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including taps having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal, wherein the equalization implementation circuitry operates on the received data signal;

programmable circuitry for allowing a first selection between integer spacing and fractional spacing to be specified;

processing circuitry for computing a second selection between integer spacing and fractional spacing; and

selection circuitry for selecting one of the first and second selections as the selected one of integer spacing and fractional spacing, wherein the selection circuitry is controlled by a programmable element to select only once while the equalization implementation circuitry operates on the received data signal.

9. (original) The circuitry defined in claim 8 wherein the selection circuitry is programmable to make its selection.

10. (original) The circuitry defined in claim 8 wherein the processing circuitry performs an algorithm to compute the second selection.

11. (original) The circuitry defined in claim 8 wherein the fractional spacing is a selectable fraction of the symbol period, wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction.

12. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including at least one selectable coefficient value;

first processing circuitry for computing the coefficient value using a selectable starting value, wherein the coefficient value is different from the starting value;

programmable circuitry for allowing a first starting value to be specified;

second processing circuitry for computing a second starting value; and

selection circuitry for selecting one of the first and second starting values as the selectable starting value, wherein the selection circuitry is controlled by a programmable element.

13. (original) The circuitry defined in claim 12 wherein the selection circuitry is programmable to make its selection.

14. (original) The circuitry defined in claim 12 wherein the first processing circuitry performs an algorithm to compute the coefficient value.

15. (original) The circuitry defined in claim 12 wherein the second processing circuitry performs an algorithm to compute the second starting value.

16. (original) The circuitry defined in claim 12 further comprising:

further programmable circuitry for allowing selection between (1) operation of the first processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

17. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including at least one selectable coefficient value;

processing circuitry for computing the coefficient value, wherein the processing circuitry receives a starting value and uses the starting value to compute the coefficient value different from the starting value; and

programmable circuitry for allowing selection between (1) operation of the processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

18. (currently amended) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry responsive to an error signal, wherein the equalization implementation circuitry operates on the received data signal;

first processing circuitry for computing a first decision directed error signal;

second processing circuitry for computing a second error signal using a training pattern; and

selection circuitry for selecting one of the first and second error signals as the error signal, wherein the selection circuitry is programmed to select only once while the equalization implementation circuitry operates on the received data signal.

19. (original) The circuitry defined in claim 18 wherein the selection circuitry is programmable to make its selection.

20. (original) The circuitry defined in claim 18 wherein the first processing circuitry performs an algorithm to compute the first decision directed error signal.

21. (original) The circuitry defined in claim 18 wherein the second processing circuitry performs an algorithm to compute the second error signal using a training pattern.

22. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

processing circuitry for computing an error signal using a selectable training pattern, wherein the processing circuitry operates on the received data signal;

programmable circuitry for allowing a first training pattern to be specified;

training pattern circuitry for providing a second training pattern; and

selection circuitry for selecting one of the first and second training patterns as the selectable training pattern, wherein the selection circuitry is programmed to select only once while the processing circuitry operates on the received data signal.

23. (original) The circuitry defined in claim 22 wherein the selection circuitry is programmable to make its selection.

24. (previously presented) Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry having at least one sampling point with a selectable location relative to a bit period of the received signal, wherein the equalization implementation circuitry operates on the received data signal;

programmable circuitry for allowing a first location of the sampling point to be specified;

processing circuitry for computing a second location of the sampling point; and

selection circuitry for selecting one of the first and second locations as the selectable location, wherein the selection circuitry is controlled by a programmable element to select only once while the equalization implementation circuitry operates on the received data signal.

25. (original) The circuitry defined in claim 24 wherein the selection circuitry is programmable to make its selection.

26. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a number of taps to be used in equalization implementation circuitry of the device operating on a received data signal from one of a programmably specified number of taps and a computed number of taps, wherein the selecting selects the number of taps only once while the equalization implementation circuitry operates on the received data signal; and

controlling the equalization implementation circuitry to operate with the number of taps selected in the selecting.

27. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a tap spacing to be used in equalization implementation circuitry of the device operating on a received data signal from one of a programmably specified tap spacing

and a computed tap spacing, wherein the selecting selects the tap spacing only once while the equalization implementation circuitry operates on the received data signal; and

controlling the equalization implementation circuitry to operate with the tap spacing selected in the selecting.

28. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a starting value for determination of a coefficient to be used in equalization implementation circuitry of the device operating on a received data signal from one of a programmably specified starting value and a computed starting value, wherein the selecting selects the starting value only once while the equalization implementation circuitry operates on the received data signal;

using the starting value selected in the selecting to determine the coefficient, wherein a value of the coefficient is different from the selected starting value; and

operating the equalization implementation circuitry using the coefficient determined in the using.

29. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting whether a coefficient to be used in equalization implementation circuitry of the device operating on a received data signal is to be determined once or on an on-going basis, wherein the selecting selects only once while the

equalization implementation circuitry operates on the received data signal; and

determining the coefficient in accordance with the selecting.

30. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting an error signal from one of a decision directed error signal and an error signal produced using a training signal, wherein the selecting selects the error signal only once while equalization implementation circuitry operates on a received data signal; and

using the error signal selected in the selecting in a determination of at least one operating parameter of the equalization implementation circuitry of the device.

31. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a training pattern from one of a programmably specified training pattern and a predetermined training pattern, wherein the selecting selects a training pattern only once while equalization implementation circuitry operates on a received data signal;

determining an error signal using the training pattern selected in the selecting; and

using the error signal in a determination of at least one operating parameter of the equalization implementation circuitry of the device.

32. (previously presented) A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a sampling location to be used in equalization implementation circuitry of the device operating on a received data signal from one of a programmably specified sampling location and a computed sampling location, wherein the selecting selects the sampling location only once while the equalization implementation circuitry operates on the received data signal; and

operating the equalization implementation circuitry using the sampling location selected in the selecting.